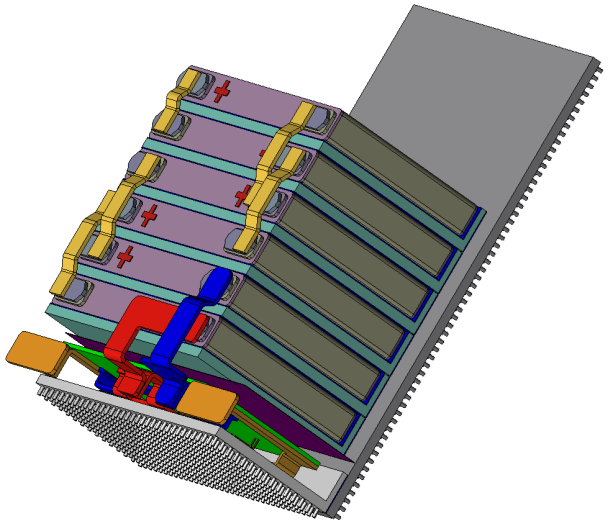


Beyond DC Assumptions:
Design Optimization of Battery Cell Interconnects Based on Transient Current Redistribution

David Morisco
Robert Bosch GmbH
Advance System Engineering – Power Trains



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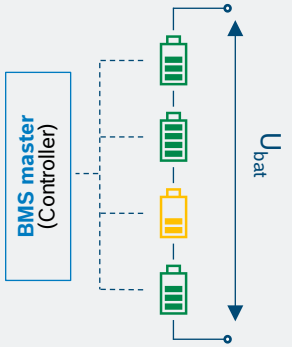
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Design Optimization of Battery Cell Interconnects
Multilevel Battery Technology

Conventional System Architecture

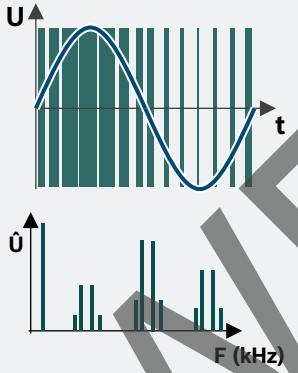
Battery (DC)



Inverter | Charger

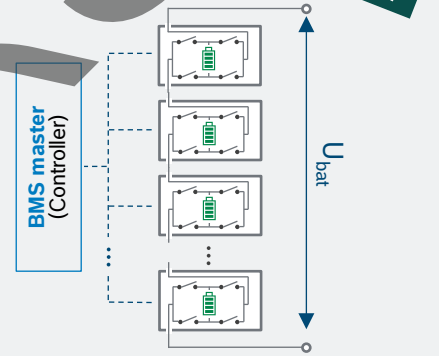


AC Output

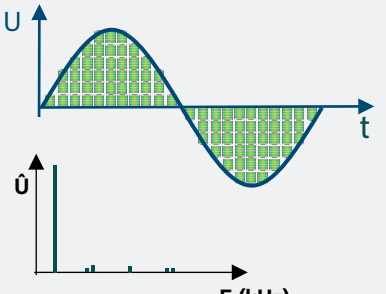


SoftwaredefinedPower (Multilevel Battery)

Battery (AC)



AC Output



SdP: Variable voltage

AC battery | direct inverter

Implications of Distributed Cell-Level Switching

System-Level Benefit

- Smaller motor-voltage steps
- Heavily reduced high-frequency voltage content

Local Design Challenge

- Fast current commutation within each cell unit
- Transient voltage stress on the MOSFETs

➢ **Main focus:** Transient current redistribution in the cell interconnect and its impact on MOSFET voltage stress

➢ **System-level implication:** Influence of the synthesized voltage waveform on electric machine losses

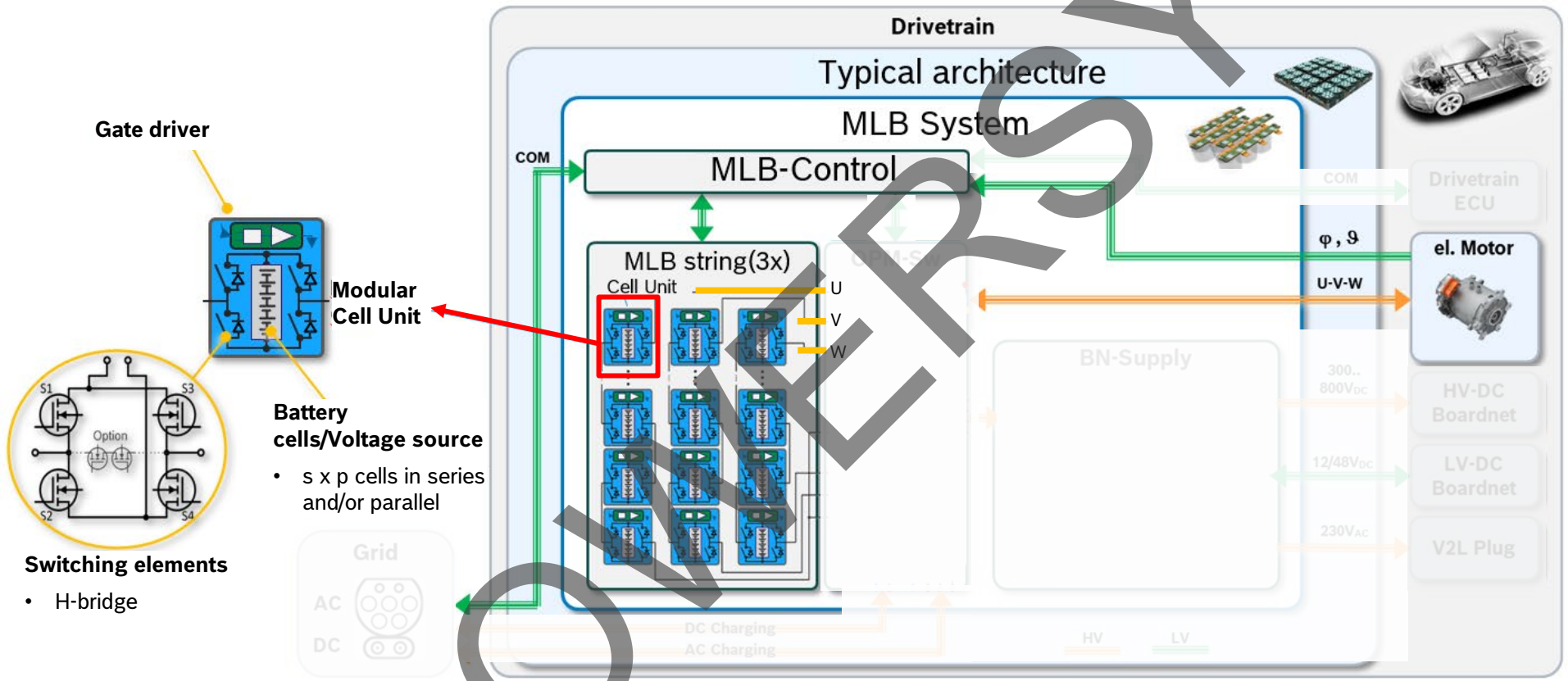
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Design Optimization of Battery Cell Interconnects

Multilevel Battery Architecture and Cell Unit



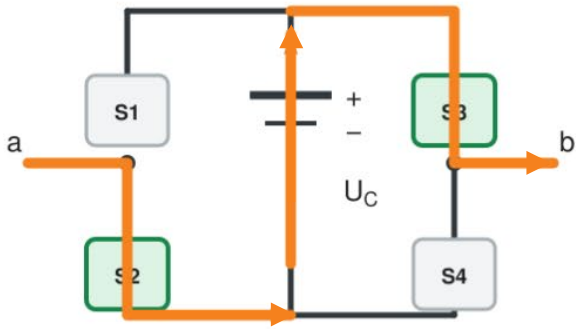
- **Voltage transition:** Current commutation within one or more cell units
- **Consequence:** The cell interconnect forms part of the transient commutation loop → geometry affect switching-device voltage stress.

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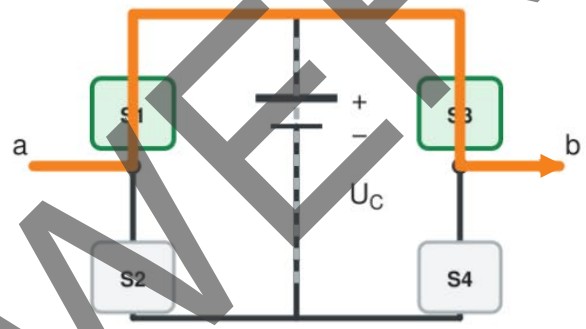
Design Optimization of Battery Cell Interconnects
Cell Unit Switching States

With $u_{unit} = v_b - v_a$, each cell unit contributes $\{+U_C, 0, -U_C\}$ to the phase voltage

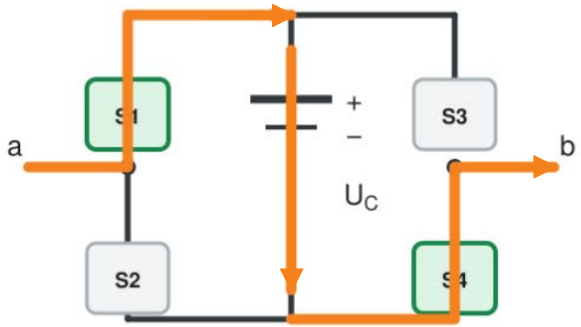
Positive insertion
$u_{unit} = +U_C$
S2 and S3 conducting



Bypass
$u_{unit} = 0$
Upper zero state: S1 and S3 conducting



Negative insertion
$u_{unit} = -U_C$
S1 and S4 conducting



Current path | conducting switch | blocked switch

- **Voltage transition:** The conducting branch changes while the phase current remains continuous
- **Consequence:** Current redistributes inside the cell interconnect and creates a transient commutation loop

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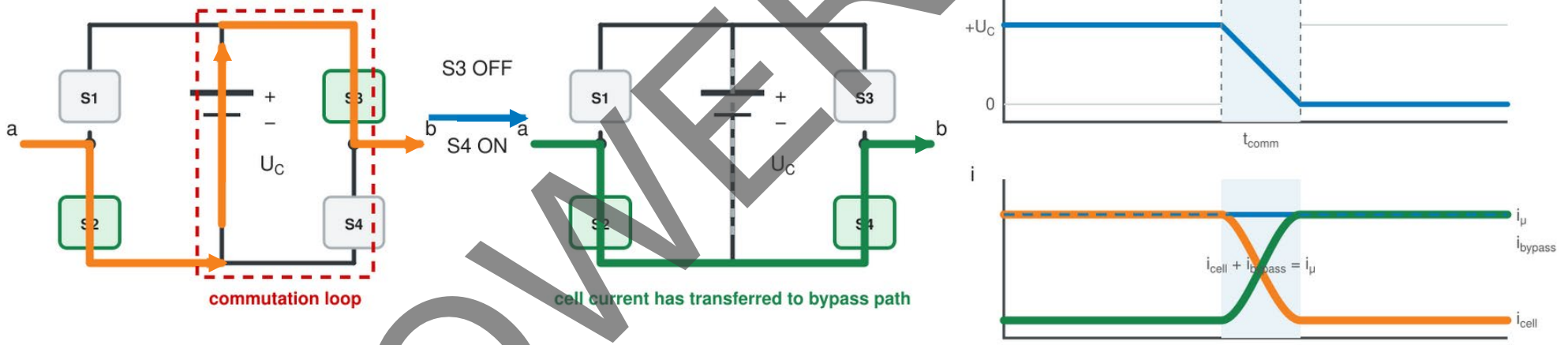
Design Optimization of Battery Cell Interconnects
Current Commutation During a Cell Voltage Step

Example: $+U_C$ to 0 using the lower bypass state, with $i_\mu > 0$ from a to b

Before switching
$u_{unit} = +U_C$ | S2 and S3 conducting

After switching
$u_{unit} = 0$ | S2 and S4 conducting

Transient redistribution
Schematic waveforms during the commutation interval



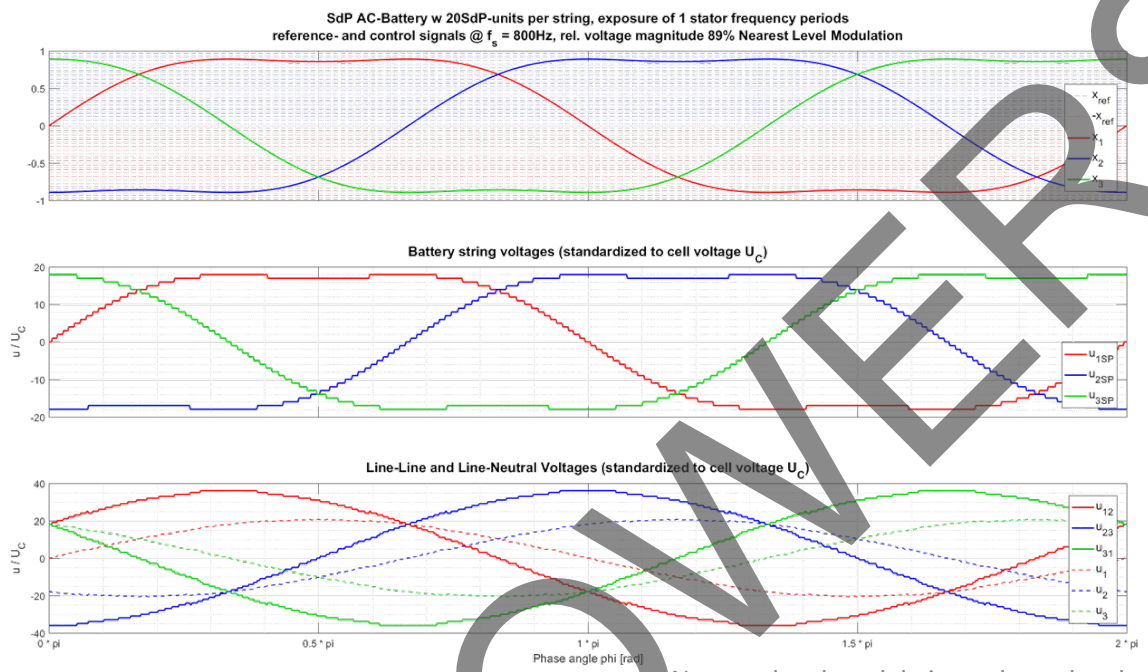
Rapid flux-linkage change produces induced voltage: $|u_{ind}|=|d\Psi/dt|$

- **Physical mechanism:** Phase current remains continuous while cell bypass currents exchange
- **Magnetic response:** Local current redistribution changes the magnetic field and the flux linkage of the commutation loop.
- **Design consequence:** Interconnect geometry and eddy currents govern flux-linkage change and MOSFET voltage stress

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Design Optimization of Battery Cell Interconnects
Near-Sinusoidal Voltage Synthesis with NLM

Example: 20 cell units per string, voltages normalized to the cell voltage U_C



NLM Principle

The controller selects how many cell units are inserted and with which polarity

Discrete voltage levels

Each state change modifies the string voltage by one cell-voltage level U_C

Result

Many small voltage steps closely follow the sinusoidal reference.

Line-to-line voltage provides even more available levels

Nearest-level modulation selects the closest available discrete voltage level at each instant.

- **System-level benefit:** Near-sinusoidal motor voltage with small voltage steps
- **Local consequence:** Every voltage step requires current commutation with a cell unit

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Design Optimization of Battery Cell Interconnects

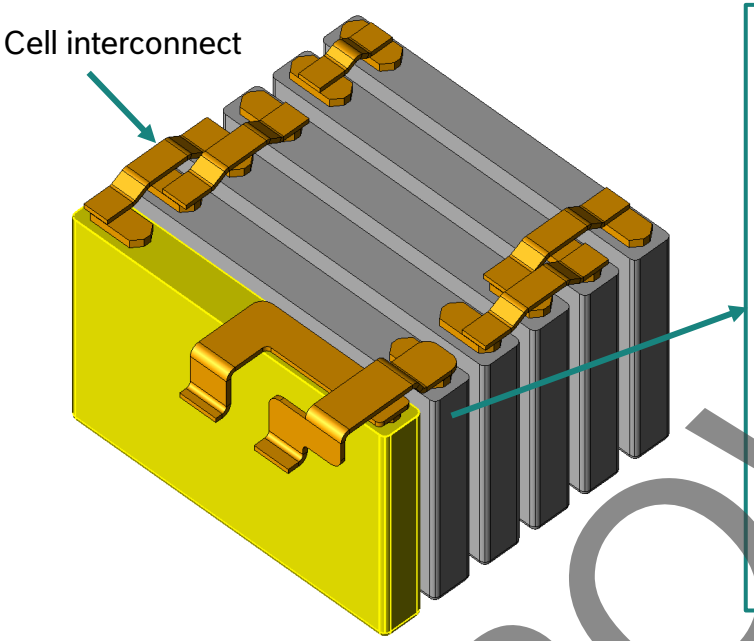
Transient 3D Model of the Six-Cell Block

FEA model size: ~25 million DOF

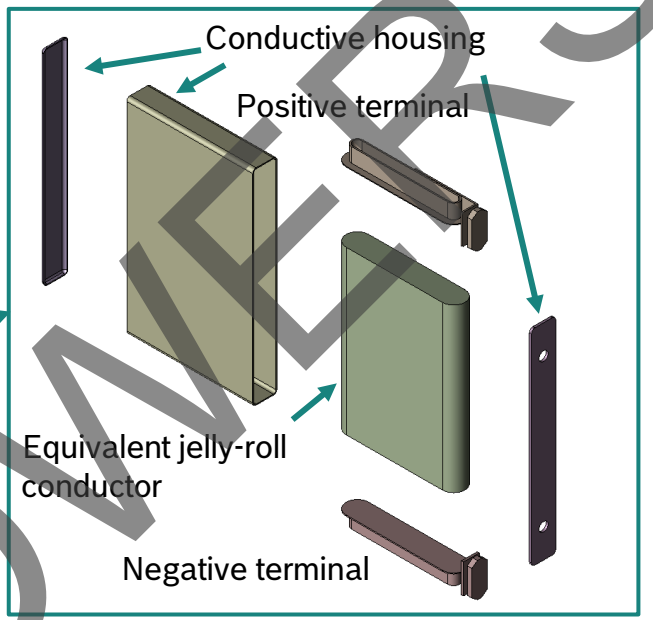
Computing performance: ~2 days per configuration using 256 CPU cores on the Bosch HPC system

Evaluated quantities: Terminal voltage, current density, magnetic flux density and transient change in flux linkage

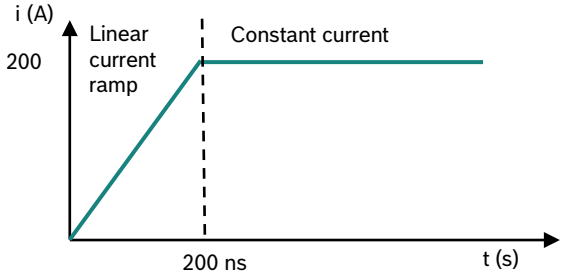
Reference configuration



Common cell model



Current excitation



- Transient eddy-current analysis
- Conductive cell and interconnect components included
- Capacitive effects neglected

➢ The model resolves the conductive cell components and interconnects that govern transient current redistribution and magnetic-field decay

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Design Optimization of Battery Cell Interconnects

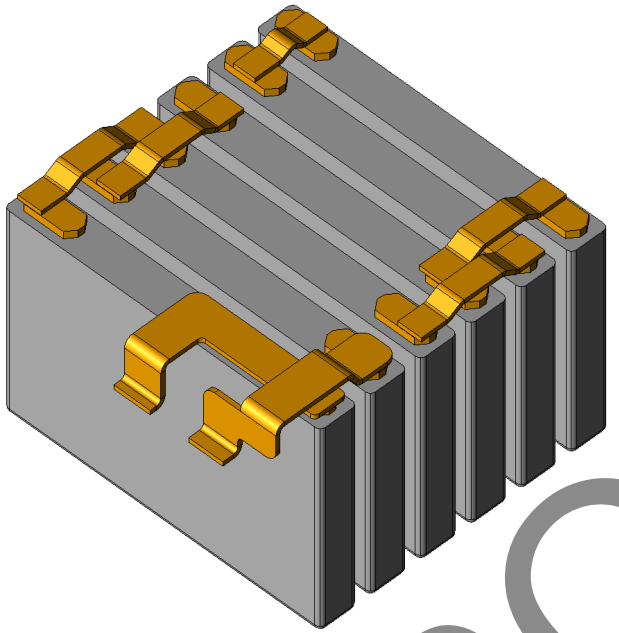
Interconnect Topologies and Design Hypotheses

Common basis: Identical cell models, materials, current excitation and evaluation method

Yellow highlighting: Modified or added conductive components

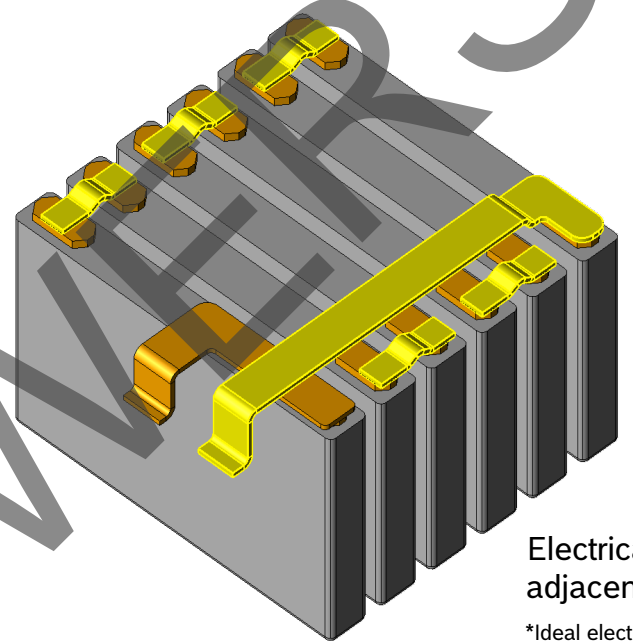
Reference configuration

Conventional cell arrangement and interconnect routing



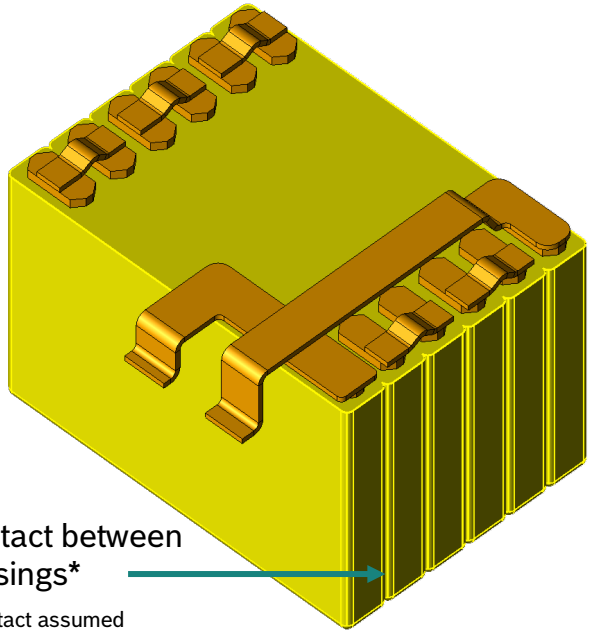
Modified interconnect routing

Reduced separation of current paths



Electrically Connected Cell Housings

Eddy-current path across the complete cell block



*Ideal electrical contact assumed

Design hypotheses:

H1 – Compact interconnect routing: Reduced effective commutation-loop flux linkage

H2 – Electrically connected housings: Slower magnetic-flux redistribution through block-wide eddy currents

➢ **Expected effect:** Lower peak induced voltage during fast current redistribution

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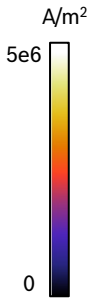
Design Optimization of Battery Cell Interconnects

Eddy-Current Density at the End of the Current Ramp

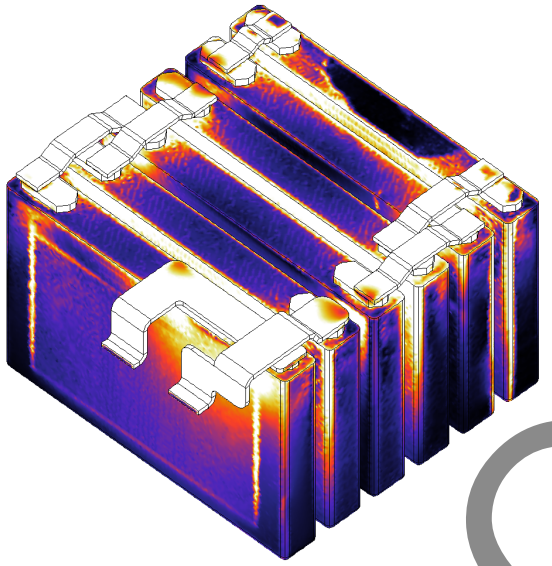
Evaluation point: End of current ramp, i = 200 A at t = 200 ns

Comparison basis: Identical eddy-current-density scale for all configurations

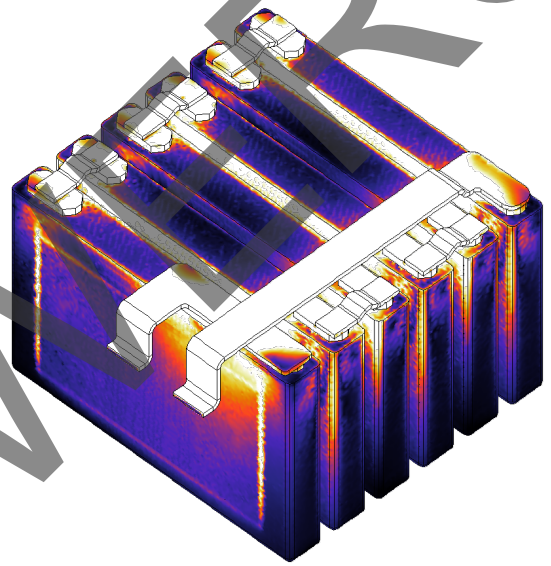
Physical origin: Changing magnetic field creates an electric field that drives currents in conductive cell components.



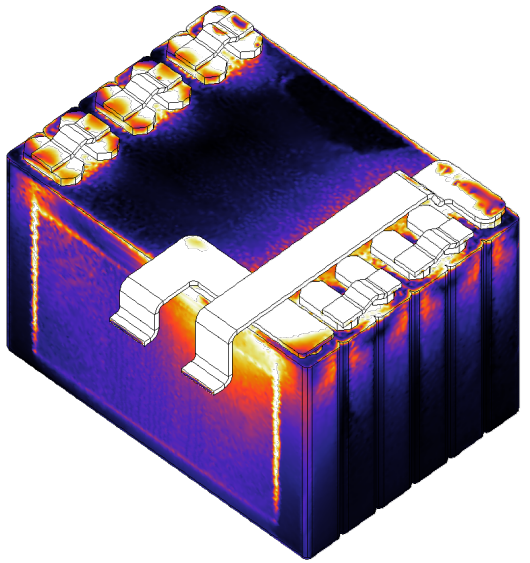
Reference configuration



Modified interconnect routing



Electrically Connected Cell Housings



➢ Interconnect geometry and housing connectivity determine the paths and spatial distribution of the resulting eddy currents.

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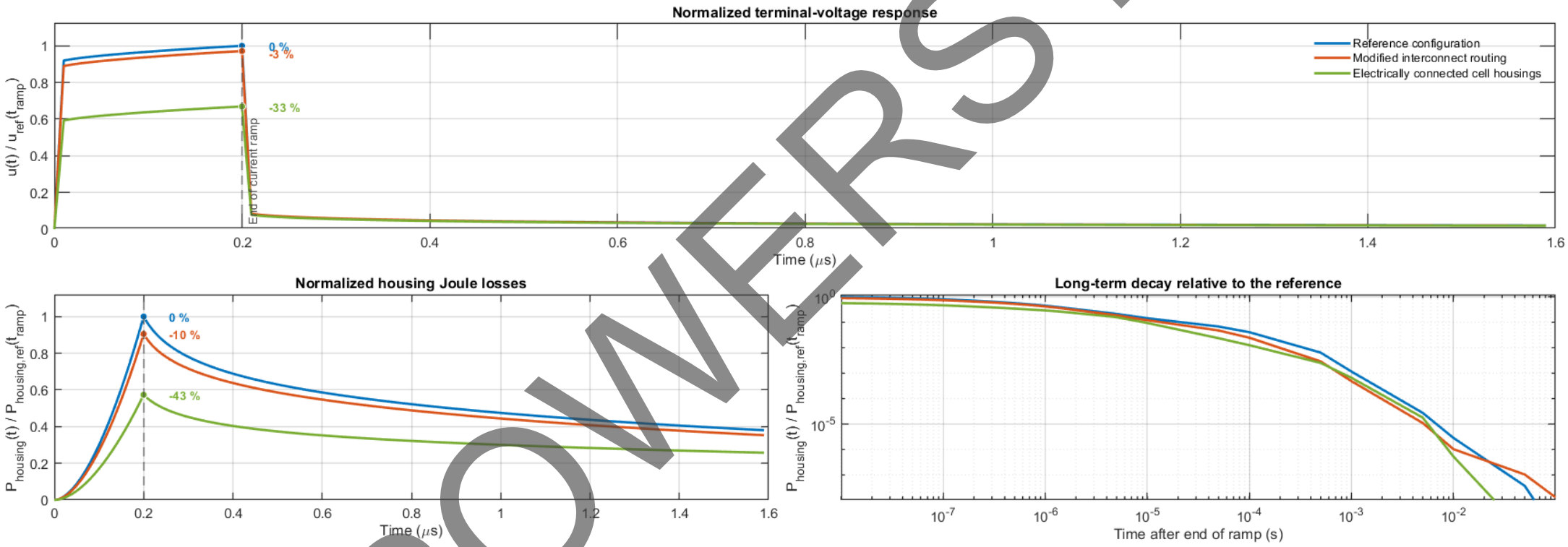
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Design Optimization of Battery Cell Interconnects

Transient Terminal-Voltage Response and Housing Joule Losses

Common excitation: Linear current ramp from 0 to 200 A in 200 ns

Normalization: Voltage and housing Joule losses normalized to the corresponding reference value at t=200ns



➢ Electrically connected cell housings reduce the terminal-voltage peak by 33% and the peak housing Joule loss by 43% relative to the reference.

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Design Optimization of Battery Cell Interconnects

Design Implications for Commutation-Robust Cell Interconnects

Scope: Investigated six-cell block with 200 ns current ramp

Geometry and electrical connectivity → **Flux linkage and eddy-current paths** → **Terminal-voltage stress and Joule losses**

1. Commutation path

Reduce commutation-loop flux linkage

- Route forward and return paths close together
- Minimize the enclosed loop area
- Consider the complete three-dimensional current path

$$|u_{\mathrm{ind}}| = \left|\frac{\mathrm{d}\lambda}{\mathrm{d}t}\right|$$

2. Conductive surroundings

Control housing connectivity

- Electrical contact creates block-wide eddy-current paths
- Treat housing contact and insulation states as design parameters

Connected-housing configuration

Terminal voltage at ramp end: **-33%**

Housing Joule loss at ramp end: **-43%**

Electrical isolation, fault behavior and manufacturability require separate assessment.

3. Evaluation method

Use transient 3D electromagnetic analysis

- Terminal-voltage peak
- Spatial eddy-current-density distribution
- Housing Joule-loss magnitude and decay

$$\nabla \times (\nu \nabla \times \mathbf{A}) + \sigma \left(\frac{\partial \mathbf{A}}{\partial t} + \nabla \phi\right) = \mathbf{J}_{\mathrm{s}}$$

DC resistance alone cannot represent the transient response.

➢ Transient commutation behavior is governed by the complete conductive cell block, not only by the nominal interconnect path.

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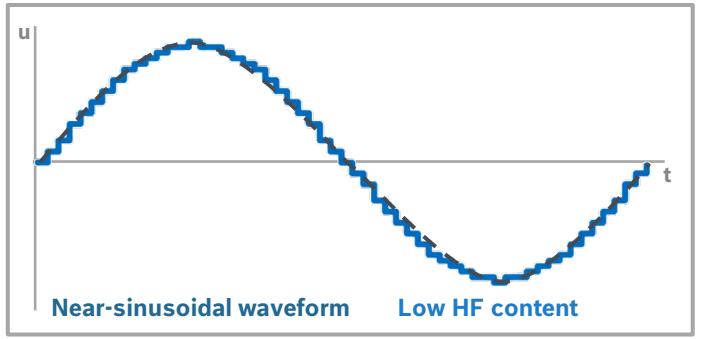
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Design Optimization of Battery Cell Interconnects
From Battery Output Voltage to Electric-Machine Excitation

FEA model size: ~135.000 DOF

Computing performance: ~300.000 time-steps in ~2–3 days per operating point using 64 CPU cores on the Bosch HPC system

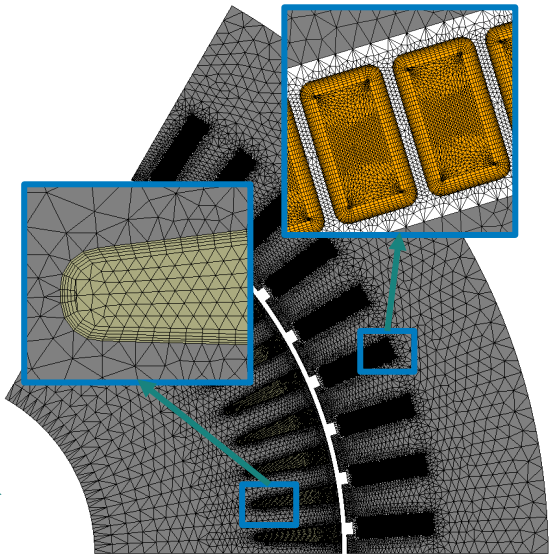
Multilevel Battery Voltage



Conventional Two-Level PWM Voltage



Induction Machine Model



Same fundamental component
Different high-frequency voltage content

Machine excitation

High-frequency voltage components cause **additional losses in the stator winding, rotor cage and iron core**

➢ The battery output voltage directly excites the electric machine and therefore influences system-level efficiency.

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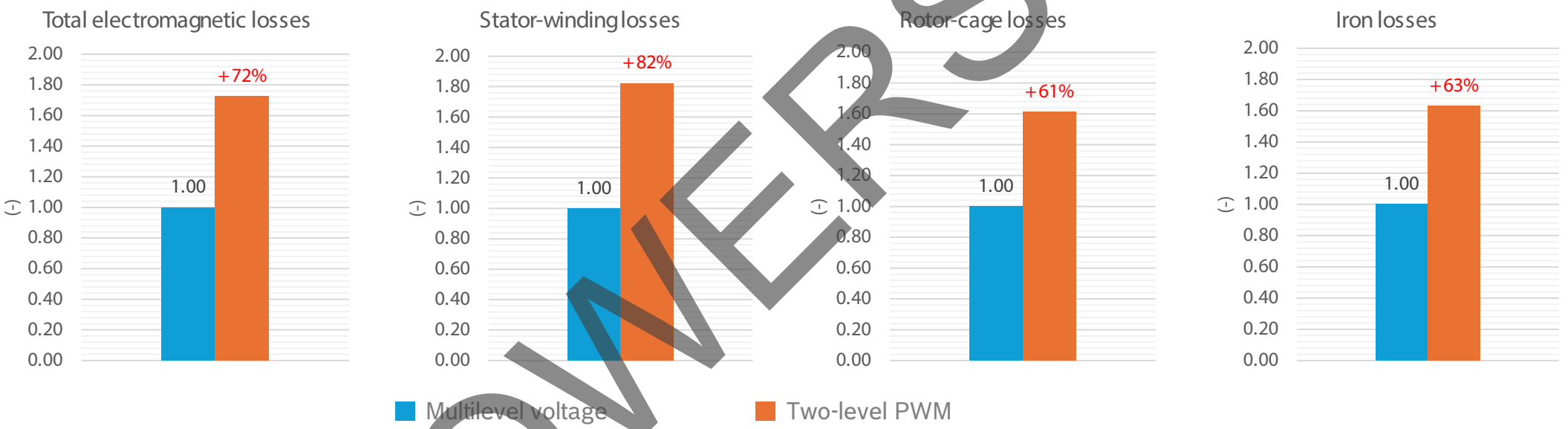
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Design Optimization of Battery Cell Interconnects

Influence of Voltage Waveform on Induction-Machine Losses

Evaluation point: Same fundamental component of excitation voltage, same temperature and material properties, same operating point

Normalization: Each loss component is normalized to the corresponding multilevel result =1.00



➢ At identical fundamental voltage and operating point, two-level PWM increases total electromagnetic losses by 72 %, mainly due to additional harmonic currents.

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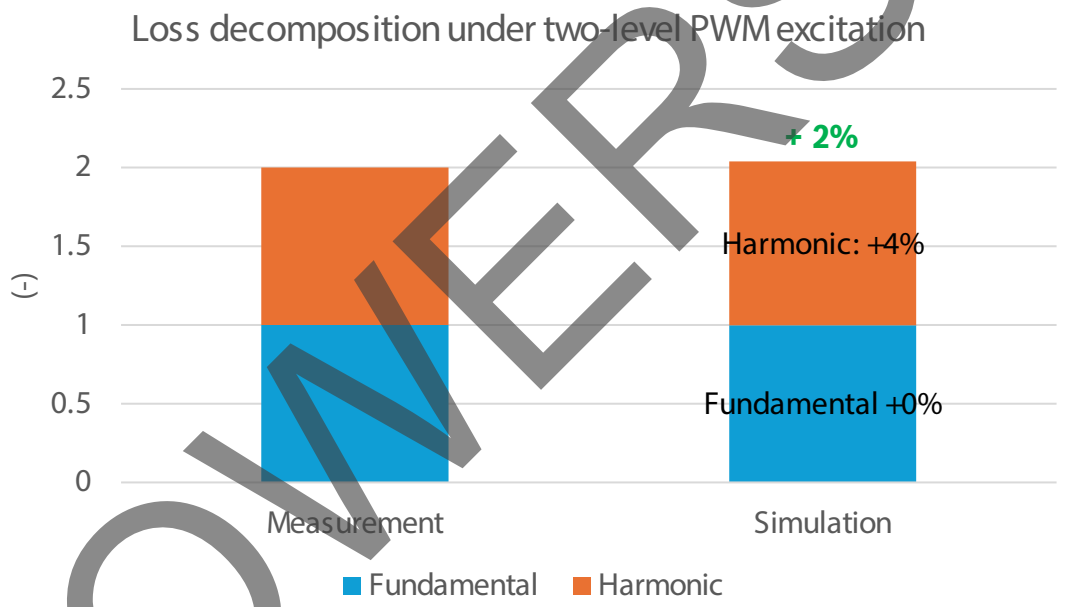
Design Optimization of Battery Cell Interconnects

Comparison with Measured Fundamental and Harmonic Losses

Evaluated excitation: Two-level PWM

Normalization: All values are normalized to the measured fundamental loss = 1.00

Comparison conditions: Same operating point, fundamental voltage component and component temperatures



Loss separation:

$P_{harmonic} = P_{EM,total} - P_{fundamental}$

No measurement-based separation into winding, rotor-cage and iron losses

- For two-level PWM excitation, harmonic losses are of the same order as the fundamental losses.
- The simulation reproduces the measured total electromagnetic losses within 2 %.

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Design Optimization of Battery Cell Interconnects
Conclusions and Design Implications

1. **Transient behavior**

> **Fast cell-level switching causes geometry-dependent current redistribution, eddy currents and induced voltage stress.**
> DC-based interconnect evaluation cannot capture these effects

2. **Interconnect design**

> **The connected-housing configuration reduced the ramp-end terminal voltage by 33% and the housing Joule-loss peak by 43%.**
> Transient 3D analysis reveals geometry-dependent current paths and decay behavior that a DC evaluation cannot capture.

3. **System-level impact**

> **The multilevel battery generates a near-sinusoidal machine voltage with low high-frequency content.**
> Two-level PWM increased the simulated electromagnetic machine losses by 72%.
> The measured and simulated total losses agreed within 2%.

➢ Transient-aware interconnect design can limit local semiconductor voltage stress, while multilevel voltage synthesis reduces high-frequency machine excitation.

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Design Optimization of Battery Cell Interconnects

Thank you for your attention

Questions?

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